



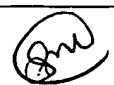
UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,234	09/30/2003	Richard H. Breinlinger	SAA-65-1	1579
23569	7590	08/31/2005	EXAMINER	
SQUARE D COMPANY INTELLECTUAL PROPERTY DEPARTMENT 1415 SOUTH ROSELLE ROAD PALATINE, IL 60067			JAGAN, MIRELLYS	
			ART UNIT	PAPER NUMBER
			2859	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,234	BREINLINGER, RICHARD H.	
	Examiner	Art Unit	
	Mirellys Jagan	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21,23-30 and 32-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 21,24-26,34 and 36-39 is/are allowed.
- 6) ☒ Claim(s) 28 is/are rejected.
- 7) ☒ Claim(s) 23,27,29,30,32,33 and 35 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 23, 29, 30, 32, 33, and 35 are objected to because of the following informalities:

In claim 23, --unit-- should be added after “processor”.

Claim 29 claims two separate ‘means’ of the system: 1) a “means for measuring” the voltages across the diode, and 2) a “means for sequentially digitizing” the analog voltage measurements. The specification discloses that the A/D converter is the means for performing both of these functions, i.e., is the element that measures the voltages across the diode and sequentially digitizes the analog voltage measurements. Therefore, the claim is not clear since it appears to state that there are two A/D converters: one as the ‘means’ for measuring the voltages and one as the ‘means’ for digitizing.

In claim 33, it is not clear how the processor unit can be ‘hosted’ by two different elements, i.e., by the controller (see claim 29) and the I/O module of claim 33, since claim 29 states that the controller hosts the processor unit, whereas claim 32 states that the I/O module is external to the controller.

In claim 35, “the current source” should be changed to --the processor--, since claim 34 states that the controller sends the control signal to the processor.

Claims 30 and 32 are objected to for being dependent on an objected base claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 28 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,554,469 to Thomson et al [hereinafter Thomson].

Thomson discloses a method comprising:

controlling a current source (12) such that the source sequentially applies a first current (I1) to a diode (10) at a first point in time, and applies a second current (I3) to the diode (10) at a second point in time;

measuring a first analog voltage (V_{be1}) across the diode when the first current (I1) is applied to the diode in order to produce a first analog voltage measurement (ΔV_{be1});

measuring a second analog voltage (V_{be3}) across the diode when the second current (I3) is applied to the diode in order to produce a second analog voltage measurement (ΔV_{be2});

sequentially digitizing the first (ΔV_{be1}) and second (ΔV_{be2}) analog voltage measurements in an integrated circuit (20) comprising an A/D converter (24);

determining a temperature proximate the diode based on the first and second digitized voltage measurements; and

Art Unit: 2859

providing a controller (not shown) hosting a processor unit (26) for controlling the current source and determining the temperature proximate the diode (see figures 1 and 4; column 2, lines 59-63; column 4, lines 35-59; and column 5, lines 1-6).

Allowable Subject Matter

4. Claims 21, 24-26, 34, 36-39 are allowed.
5. Claims 23, 27, 29, 30, 32, 33, and 35 would be allowable if amended to overcome the objections set forth in this Office action.

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not disclose or suggest the following in combination with the remaining limitations of the claims:

A system for automated temperature measurement comprising a processor unit configured to obtain a digital measure of a first voltage across the diode from the converter when the first current is applied to the diode, and obtain a digital measure of a second voltage across the diode from the converter when the second current is applied to the diode; and a controller configured to host the processor unit (see independent claim 21).

A system for automated temperature measurement comprising means for sequentially digitizing the first and second analog voltages measurements with an integrated circuit and a processor for determining a temperature based on the first and second digitized voltage

Art Unit: 2859

measurements; and a controller configured to host the processor unit and the means for controlling the current source (see independent claim 29).

A networked system for automated temperature measurement comprising an A/D converter for converting the first voltage to a first digital signal and the second voltage to a second digital signal, and a processor for determining a temperature based on the first and second digital signals; and a controller connected to the network at a second location and configured to provide a control signal and receive a temperature signal as claimed (see independent claim 34).

Response to Arguments

7. Applicant's arguments that claim 28 is patentable over Thomson because it has similar limitations as those in allowable claims 21 and 29, i.e., that the limitations of “sequentially digitizing the first and second analog voltage measurements in an integrated circuit comprising an analog-to-digital converter” and “providing a controller hosting a processor unit for controlling the current source and determining the temperature proximate the diode” are similar limitations to those in claims 21 and 29, have been considered but are not persuasive.

Claim 21 claims that the processor unit obtains “a digital measure of a first voltage across the diode from the analog-to-digital converter when the first current is applied to the diode” and “a digital measure of a second voltage across the diode from the analog-to-digital converter when the second current is applied to the diode”.

Claim 29 claims that the system has “means for measuring a first analog voltage across the diode when the first current is applied to the diode and for measuring a second analog voltage

Art Unit: 2859

across the diode when the second current is applied to the diode” and “means for sequentially digitizing the first and second analog voltage measurements”.

Claim 28 states “measuring a first analog voltage across the diode when the first current is applied to the diode to produce a first analog voltage measurement; measuring a second analog voltage across the diode when the second current is applied to the diode to produce a second analog voltage measurement”, and “sequentially digitizing the first and second analog voltage measurements in an integrated circuit comprising an analog-to-digital converter”.

In Thomson, a first current (I_1) is applied to the diode (10) and a resulting voltage across the diode (V_{be1}) is measured and held by the signal conditioner (22), then second current (I_2) is applied across the diode and the resulting voltage across the diode (V_{be2}) is obtained by the signal conditioner (22). The signal conditioner (22) then uses the voltages (V_{be1} and V_{be2}) to produce a first analog voltage measurement (ΔV_{be1}) that is then digitized by the A/D converter (24) and sent to and held by the register (28) in the processor unit. A third current (I_3) is then applied to the diode (10) and a resulting voltage across the diode (V_{be3}) is measured and held by the signal conditioner (22), then another current (I_4) is applied across the diode and the resulting voltage across the diode (V_{be4}) is obtained by the signal conditioner (22). The signal conditioner (22) then uses the voltages (V_{be3} and V_{be4}) to produce a second analog voltage measurement (ΔV_{be2}) that is then digitized by the A/D converter (24) and sent to the register (28) in the processor unit. The register (28) then uses the digitized voltage measurements (ΔV_{be1} and ΔV_{be2}) to calculate the temperature (T).

Therefore, Thomson does not anticipate claim 21 because he does not obtain a digital measure of the voltage across the diode from the A/D converter, but instead obtains from the

Art Unit: 2859

A/D converter a digital value of the differences in voltages (e.g., digitized values of ΔV_{be1} and ΔV_{be2}) across the diode.

Furthermore, Thomson does not anticipate claim 29 because he does not have means for sequentially digitizing the first and second analog voltages, and a processor unit for determining a temperature based on the digitized voltages, but instead has means for sequentially digitizing the differences in voltages (e.g., A/D digitizes the voltage differences ΔV_{be1} and ΔV_{be2} across the diode, not the analog voltages V_{be1} and V_{be2}), and a processor unit for determining a temperature based on the digitized voltage differences ΔV_{be1} and ΔV_{be2} , not on digitized values of V_{be1} and V_{be2} .

However, Thomson does anticipate claim 28 because he measures a first analog voltage across the diode (e.g., V_{be1} or V_{be2}) when the first current (e.g., I_1 or I_2) is applied to the diode to produce a first analog voltage measurement (e.g., ΔV_{be1}); measures a second analog voltage across the diode (e.g., V_{be3} or V_{be4}) when a second current (e.g., I_3 or I_4) is applied to the diode to produce a second analog voltage measurement (e.g., ΔV_{be2}), and sequentially digitizes the first (e.g., ΔV_{be1}) and second (e.g., ΔV_{be2}) analog voltage measurements in an integrated circuit comprising an analog-to-digital converter. The processor unit then determines temperature based on the digitized first and second voltage measurements (e.g., based on the digitized values of ΔV_{be1} and ΔV_{be2} sequentially received by the register 28).

Conclusion

Art Unit: 2859

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mirellys Jagan whose telephone number is 571-272-2247. The examiner can normally be reached on Monday-Friday from 11AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2859

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MJ

August 23, 2005

G. Verbitsky
GAIL VERBITSKY
PRIMARY EXAMINER